REMARKS

Applicant has reviewed and considered the Office Action mailed on August 13, 2003, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-36 are now pending in this application.

Applicant has renumbered dependent claim 30 as claim 31 as directed by the Examiner. Applicant thanks the Examiner for bringing this to Applicant's attention.

§103 Rejection of the Claims

Claims 1-36 were rejected under 35 USC § 103(a) as being unpatentable over Madhaven et al. (U.S. Patent No. 5,675,545) in view of Ho (U.S. Patent No. 6,421,814). Applicant respectfully traverses these grounds for rejection.

Claim 1, in part, recites "a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure," and "changes of global geometric variables in the global file may cause changes in the design cells for the physical layout of the hierarchical semiconductor structure."

Applicant can not find in Madhaven et al. (hereafter Madhaven) a teaching or suggestion of geometric variables related to the physical layout of a hierarchical semiconductor structure or a teaching or suggestion for changing a design cell for the physical layout of the hierarchical semiconductor structure, as recited in claim 1. The Examiner apparently agrees stating "Madhaven does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed." Further, Applicant can not find a teaching or suggestion in Madhaven regarding a "hierarchical semiconductor structure." Madhaven's hierarchical methods deal with interconnections between circuit blocks. *See Madhaven, Abstract and Summary, in particular, column 2, lines 1-8, and column 7, lines 16-17.* Hierarchically interconnecting circuit blocks is distinctly different that changing a design cell for the physical layout of the hierarchical semiconductor structure, as recited in claim 1. Further, Madhaven discusses a methodology of a software tool where "[t]he methodology of the software tool to combine the various conductivity data (information) in the memory block and BIST interface as a physical schematic diagram is illustrated in Fig 10 to implement a memory module." *See*

Madhaven, column 7, lines 37-40. In addition to the normal definition of a physical schematic diagram, review of Madhaven's Figure 10 demonstrates that a physical schematic diagram as used in Madhaven is distinctly different than a physical layout for a semiconductor structure. Through an electronic search of Madhaven, Applicant can not find another discussion related to the term "physical," which further indicates that Madhaven does not deal with the physical layout of a hierarchical semiconductor structure.

Further, Madhaven deals with forming a database associated with circuit blocks of an integrated circuit using a built in self test (BIST) interface. *See, Madhaven, column 3, line 63-column 4, line 13.* Using a BIST interface, a circuit block can be tested to determine how the circuit block functions with respect to input test data. Thus, Madhaven deals with functionality of circuit blocks, not the physical layout of a hierarchical semiconductor structure. *See, Madhaven, column 6, lines 48-column 7, line 5.*

Applicant can not find in Ho a teaching or suggestion of geometric variables related to the physical layout of a hierarchical semiconductor structure or a teaching or suggestion for changing a design cell for the physical layout of the hierarchical semiconductor structure, as recited in claim 1. Though Ho may discuss device parameters, which may include geometric variables in a semiconductor structure, Applicant can not find in Ho a teaching or suggestion relating such device parameters in a local file to device parameters in global file in a manner as recited in claim 1. Further, Applicant can not find a teaching or suggestion in Ho regarding a hierarchical semiconductor structure, or geometric variables related to a physical layout in a hierarchical semiconductor structures. In discussions with respect to Figures 19-21, Ho refers to hierarchical blocks in an integrated circuit. *See, column 11, lines 16-28.* Reviewing this discussion and associated figures, it appears that the hierarchical process of Ho deals with a hierarchical block structure of the circuitry of an integrated circuit which is distinctly different than a hierarchical semiconductor structure. Though Ho may use geometric variables in extracting parameters relative to a hierarchical circuit layout, Applicant can not find a teaching of suggestion that Ho uses these geometric variables in a physical layout in a hierarchical semiconductor structure. Thus, Ho does not cure the above-mentioned deficiencies of Madhaven.

Since Madhaven deals with a hierarchy interconnecting circuit blocks, and Ho briefly discusses a hierarchical block structure of circuitry of an integrated circuit, the combination of Madhaven and Ho does not teach or suggest geometric variables relating to a physical layout in a hierarchical semiconductor structure, as recited in claim 1. Thus, Applicant submits that the combination of Madhaven and Ho does not teach or suggest all the elements of claim 1, and therefore, claim 1 is patentable over Madhaven in view of Ho.

Further, the combination of Madhaven with Ho is not proper since there is no suggestion to combine the cited references as proposed in the Office Action, because there is no reasonable expectation for success of the proposed combination. The Office Action states that

> "[t]his would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout file and geometrical shape variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhaven to better improve and faster layout processing in circuit design and testing as in Madhaven."

Applicant can not find a teaching or suggestion for using a geometrical layout file and geometrical shape variables in hierarchical relationships for a physical design of an integrated circuit disclosed in Madhaven as proposed in this quote. Madhaven deals with "an improved technique of assembling databases of complex circuit blocks that are being combined on a single integrated circuit chip to form a specific system architecture." *Underlining added. See, column 83, lines 47- 49.*

Further, Applicant can not find where Madhaven discloses a method and system that could use Ho's geometric variables for the physical layout of a hierarchical semiconductor structure. Combining Ho's device parameters with Madhaven's interconnection of circuit blocks approach would result in extraneous data for Madhaven's system and method, since Madhaven appears not to deal with an integrated circuit at the geometric and physical level of these geometric variables. Applicant can not find in the cited references or in the Office Action any reasons that would indicate that the Ho device parameters could be utilized in Madhaven's method and system, as proposed by the Office Action.

The Office Action stated "[p]ractitioner in the art at the time of the invention was made would have found Madhaven physical semiconductor memories in the integrated circuit area could have geometric shapes or sizes taking geometric parameter values, occupied in the chip

area such that the chip could be tested. Such geometrical feature is also well-known in the semiconductor circuit design." The fact that semiconductor memories have geometrical features does not teach or suggest that Madhaven deals with the semiconductor memories at the physical layout of a semiconductor structure level or that Madhaven's method and apparatus can use geometric variables related to the physical layout of a semiconductor structure as recited in claim 1. The Office Action has provided no objective reference or a specific reason to support the proposition that Madhaven can use Ho's geometric parameters. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. *(Underlining added.)* Since no reasonable expectation of success has been provided for the combination of Madhaven with Ho as proposed in the Office Action, Applicant submits that such combination is not proper.

For the reasons stated above, Applicant submits that claim 1 is patentable over Madhaven in view of Ho. Claims 9, 15, 22, 26, 30, and 33 recite similar elements as claim 1, and are patentable over Madhaven in view of Ho for the reasons stated above and additionally in view of the further elements recited in these independent claims.

Claims 2-8, 10-14, 16-21, 23-25, 27-29, 31-32, and 34-36 depend, directly or indirectly, on claims 1, 9, 15, 22, 26, 30, and 33, respectively, and are patentable over Madhaven in view of Ho for the reasons stated above and additionally in view of the further elements recited in these dependent claims.

Applicant respectfully requests withdrawal of these rejections of claims 1-36, and reconsideration and allowance of these claims.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

JOSEPH J. KARNIEWICZ

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2157

Date 13 November 2003 By David R. Cochran

David R. Cochran
Reg. No. 46,632

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13 day of November, 2003.

Tina Kohout
Name

Signature